REMARKS

The Office Action of February 22, 2005 has been carefully considered. Reconsideration and allowance in view of the following remarks is respectfully requested.

Claims 1-8 were rejected as being anticipated by Sakakibara. Claims 1, 2, 4, 5, 7 and 8 were rejected as being anticipated by Duboc. These rejections are respectfully traversed.

As recited in claim 1, a set of memory addresses is formed by passing a base memory address to an address configuration means, the address configuration means using the base memory address and a configuration instruction to define a set of memory addresses. This combination of features is not believed to be taught or suggested by the cited references.

In particular, in Sakakibara, each access request control unit (RQ0,...,RQ3) is provided with its own base address register (Fig. 5). There is no base memory address that is used to define a set of memory addresses as in the present invention. Rather, there is a set of base memory addresses used to define a set of memory addresses.

In Duboc, the situation is similar. Each data address generator (DAG) is provided with a set of indirect address registers (Fig. 4). For each DAG, one of these indirect address registers is selected and the contents thereof used as the address. There is no base memory address that is used to define a set of memory addresses as in the present invention.

Withdrawal of the rejections and allowance of claims 1-8 is respectfully requested.

Respectfully submitted,

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